Remarks

In view of the above amendments to the claims and following discussion, the applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U. S. C. § 102, or obvious under the provisions of 35 U. S. C. § 103. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

A. 35 U. S. C. § 102

1. Claims 1-5, 8, 11 and 13 are patentable over Koyama et al.

Claims 1-5, 8, 11 and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003). The applicants submit that these claims are not anticipated in this reference.

Claim 1 is directed to a display screen including:

light emitters (4, 6, 8) arranged as rows of light emitters and columns of light emitters to form an array of light emitters,

a silicon substrate (62) on which control means (2, 10, 20, 30, 40, 42, 44, 46, 48, 50) to control the emissions of the light emitters are fabricated, these control means including:

means (12, 22, 32) for powering the light emitters (4, 6, 8),

a plurality of addressing electrodes (40) arranged according to the columns of light emitters, and intended to transmit a voltage (V_D) representing an image datum to each column of light emitters,

a plurality of selection electrodes (42, 44, 46) arranged according to the rows of light emitters, and intended to transmit a selection signal (V_{S42}, V_{S44}) to each row of light emitters,

a plurality of modulation transistors (14, 24, 34), each associated with a light emitter of the array, the said modulation transistors including a gate electrode intended to be connected to an addressing electrode (40) and two current-carrying electrodes, each modulation transistor intended to

have a drain current pass through it to power the said light emitter for a voltage between its gate electrode and one of its current-carrying electrodes that is greater than or equal to a threshold trigger voltage (V_{th}), the said modulation transistors (14, 24, 34) being arranged in columns associated with the columns of light emitters and being geometrically aligned on the substrate (62) along a guiding line (72),

a load capacitor (16, 26, 36) connected to the terminals of each modulation transistor (14, 24, 34) and intended to set an electric potential at the gate electrode of the associated modulation transistor, and

a plurality of compensating transistors (48) intended to compensate for the threshold trigger voltage of the modulation transistors by adjusting the charge on the capacitor,

wherein a single compensating transistor (48) is connected to all the modulation transistors (14, 24, 34) of a given column and is intended to compensate for the threshold trigger voltages of all the said modulation transistors (14, 24, 34) of this column, and

wherein that the said compensating transistor (48) of a given column is formed in the geometrical extension of the line-arrangement of the said modulation transistors (14, 24, 34) of this given column along the said same guiding line (72).

In reference to FIG. 1 and 2 of the present application, that are reproduced in the table below, the applicant would emphasize the following two features:

the last claimed feature of the modulation transistors: "the modulation transistors (see ref.14, 24, 34 on the circuit of FIG. 1 and the layout on FIG. 2) of a same column of light emitters are aligned on the substrate (62) according to a guiding line (72)."

the last claimed feature of the compensating transistor: "the compensating transistor (48) of a given column is formed in the extension of the line-arrangement of the said modulation transistors (14, 24, 34) of a given column according to the said same guiding line (72)."

the modulation transistors ref.14, 24, 34 and the compensating transistor **48** are aligned

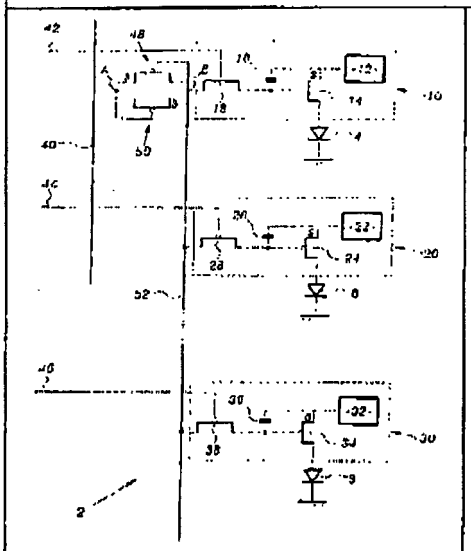

Fig.1

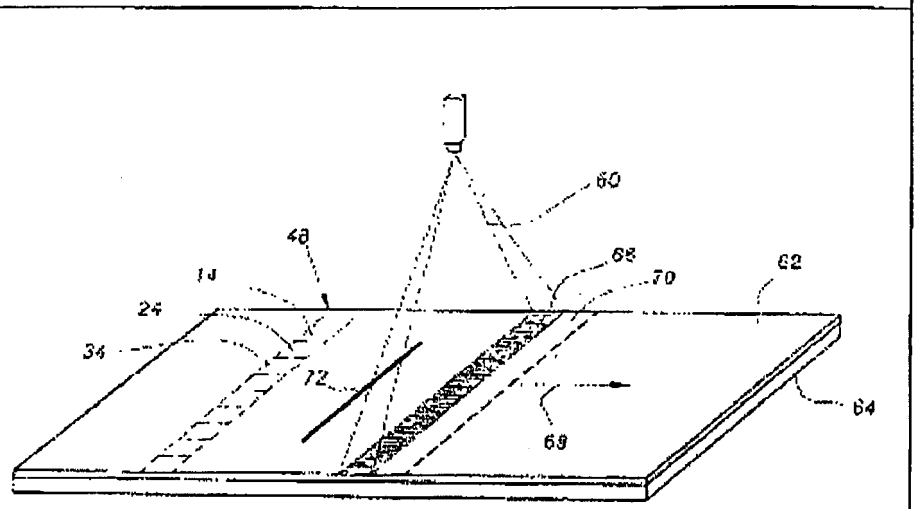

Fig.2

With regard to claim 1, the Examiner indicates that Koyama et al. discloses that the compensating transistor (TFT 114 on figures 1, 8 or TFT 914 on figure 9) is formed in the extension of the line-arrangement of the modulation transistors (TFT 102 on figure 1, TFT 902 on figure 9) of a given column according to the said same guiding line. Applicants disagree, nothing in Koyama et al. discloses or even suggest that the compensating transistor TFT 102 or 902 is aligned with all the modulation transistors TFT 114 or 914 of a same column.

Koyama et al. does not recite any of the advantages of such an alignment as recited below (see below citations of lines 17-37 at page 13 of applicant's specification):

1) "The modulation transistors 14, 24, 34 of a column ... and the compensating transistor 48 to which they are connected are formed in such a way that they are positioned one after the other in a line that is

parallel to the long sides of the heating surfaces 66"... wherein the heating surface 66 is defined in applicant's specification at page 13, lines 2-4 as a rectangular surface extending longitudinally along a guiding line 72 which is heated by a pulsed laser beam 60.

2) "these transistors (14, 24, 34 and 48) are (therefore) fabricated on one and the same heating surface 66 heated, at the same time, by the same laser beam 60.
3) Because of this alignment, "Therefore, they present threshold trigger voltages having similar values such that the compensating transistor 48 is able to compensate for the threshold trigger voltages of all the modulation transistors 14, 24, 34 of a column of light emitters".

The above passages mean that, as the compensating transistor 48 of a given column of emitters modulated by the modulation transistors 14, 24, 34 has the same threshold trigger voltage as the threshold trigger voltage of these modulation transistors 14, 24, 34, this compensating transistor 48 is very well adapted to compensate the threshold trigger voltage of these particular modulation transistors 14, 24, 34 of the same column.

Koyama et al. in paragraph 0076 and FIG. 1 only lists the different components of a pixel without any mention of geometrical alignment. Koyama et al. at FIG. 4 only illustrates columns as straight lines along the pixels are aligned. Koyama et al. does not recite any alignment for the modulators and there is no mention of the geometrical alignment of the modulators.

Koyama et al. in paragraph 0118 and FIG. 9 recites: "The portion 118 of the source signal line driving circuit is composed of a correction TFT 914." As such, the portion 118 of the source signal line driving circuit is an extension of the modulation transistor aligned to the vertical column as shown in FIG. 4 of Koyama et al. However, such an extension does not describe or suggest that "the compensating transistor (48) of a given column of light emitters is formed in the geometrical extension of the line-arrangement of the said modulation transistor of the said given column along the said same guiding line as the

guiding line along which modulation transistors of this column are aligned on the substrate", as recited in claim 1.

Also, applicant's specification from line 16 at page 15 up to line 2 at page 16, recites: "Since the modulation transistors 14 and the compensating transistor 48 have been fabricated on the same heating surface, they have similar threshold trigger voltages and $V_{th48} = V_{th14}$ ... Thus, the drain current I_d flowing through the modulation transistor 14 is independent of its threshold trigger voltage V_{th14}. The threshold trigger voltage V_{th48} of the compensating transistor 48 compensates for the threshold trigger voltage of the modulation transistor V_{th14} such that the luminance of the pixel associated with the light emitter 2 is constant for a given addressing voltage."

The last feature of the compensating transistor that is claimed in claim 1 ("the compensating transistor of a given column is formed in the extension of the line-arrangement of the said modulation transistors of a given column according to the said same guiding line") cannot be considered as an obvious matter of design, as it provides definitely the above mentioned advantage. Consequently, as claim 1 is not described in Koyama et al., claim 1 is patentable thereover. Moreover, claim 1 is not obvious over Koyama et al.

Claims 2-5, 8, 11 and13 depend directly from claim 1. In view of the above arguments, claims 2-5, 8, 11 and 13 are also patentable over Koyama et al. based on their dependence on claim 1.

B. 35 U. S. C. § 103

1. Claim 6 is patentable over Koyama et al. in view of Hatano et al.

Claim 6 stands rejected under 35 U.S.C.103(a) as being unpatentable over Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003) in view of Hatano et al. (U. S. Patent Application US 2004/0017365

published January 29, 2004). The applicants submit that this claim is not rendered obvious by the combination of these references.

Claim 6 recites that, in the display screen as claimed in claim 1:

the modulation transistors (14, 24, 34) and the associated compensating transistor (48) are fabricated on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate (62), using a laser beam (60), the said beam being intended first to heat a first rectangular heating surface (66) of the substrate, then to move in a direction of movement (68) and then to heat a second rectangular heating surface (70),

the said modulation transistors (14, 24, 34) associated with the light emitters of a given column and the associated compensating transistor are aligned in one and the same heating surface (66), the guiding alignment line (72) extending approximately perpendicularly to the direction of movement (68) of the laser beam.

As stated above, Koyama et al. does not disclose the formation, as claimed in claim 1, of compensating transistor of a given column in the extension of the line-arrangement of the modulation transistors of this given column according to the same guiding line as the guiding line according to which the modulation transistors of this given column are aligned on the substrate. Koyama et al. does not disclose the above specific features of claim 6.

Notably at paragraphs 0013, 0014, 0019 and 0024, Hatano et al. teaches indeed the formation, on an insulating substrate, of "discontinuous converted regions of roughly-band-shaped-crystal silicon films", by heating an amorphous silicon substrate using a laser beam ("irradiating pulse-modulated laser light"). "Desired circuit sections such as drive circuit sections (modulation transistors) are fabricated in these discontinuous rectangular converted regions."

However:

- Hatano et al. does not teach the formation of a compensating transistor of a given column in the extension of the line-arrangement of the modulation transistors of this given column according to the same guiding line as the

guiding line according to which the modulation transistors of this given column are aligned on the substrate, because Hatano et al. does not disclose any compensation transistor.

- When using a laser beam being intended first to heat a first rectangular heating surface of a substrate, then to move in a direction of movement and then to heat a second rectangular heating surface, in such a way that an amorphous silicon substrate is obtained from a polycrystalline silicon substrate, and that modulation transistors are fabricated, Hatano et al. does not teach the fabrication of compensating transistors, each associated with the modulation transistors of given column.
- Further, Hatano et al. does not teach that the said modulation transistors associated with the light emitters of a given column and the associated compensating transistor are aligned in one and the same heating surface, the guiding alignment line extending approximately perpendicularly to the direction of movement of the laser beam.

Consequently, claim 6 which depends on claim 1 is patentable over Koyama et al. in view of Hatano et al.

2. Claims 7 and 12 are patentable over Koyama et al.

Claims 7 and 12 stand rejected under 35 U.S.C.103(a) as being unpatentable over Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003). The applicants submit that these claims are not rendered obvious by this reference.

Claim 7 recites that, in the display screen as claimed in claim 1, the said modulation transistors and the said associated compensating transistor each include a channel between two layers of doped material, the said channel being connected to their gate electrode, and in that the channel of the modulation

transistors of a column and the channel of the associated compensating transistor have a main axis approximately parallel to the said guiding line 72. At page 13, lines 26-31 of applicant's specification, it is stated that "the modulation transistors 14, 24 and 34 and the compensating transistor 48 are produced such that their drain channel has a main axis approximately perpendicular to the direction 68 of movement of the laser beam", i.e. parallel to the said guiding line 72. Using such an orientation of the channel parallel to the guiding line 72 make it easier to insert the transistors on the rectangular surfaces 66 heated by the laser beam, because these heated rectangular surfaces 66 are narrow and may be narrower than the length of the channels to fabricate. Therefore, using such a orientation of the channel parallel to the guiding line 72 enhance still further the similarities of the threshold trigger voltage V_{th14}, ... of the modulation transistors with the threshold trigger voltage V_{th48} of the compensating transistors 48 of the same column, then providing a further enhancement of the compensation of the threshold trigger voltage V_{th14}, ... as stated in applicant's specification at page 13, lines 33-37.

With regard to claim 7, the Examiner admits that "Koyama et al. does not disclose the main axis is parallel to the guiding line". But the Examiner considers that, "At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to change the orientation of the transistors (i.e. channels) because applicants have not disclosed that the specific orientation as claimed provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a different transistor orientation because it would not have a significant, if any, impact of the performance of the circuit." The applicants strongly disagree with this statement, on the grounds developed in the previous paragraph showing the advantages of the claimed orientation.

Consequently, claims 7 and 12 which depend from claim 1 are patentable over Koyama et al.

3. Claims 9-10 are patentable over Koyama et al. in view of Lo

Claims 9-10 stand rejected under 35 U.S.C.103(a) as being unpatentable over Koyama et al. (U. S. Patent Application US 2003/0107534 published June 12, 2003) in view of Lo (U. S. Patent 6,937,215 issued August 30, 2005). The applicants submit that these claims are not rendered obvious by the combination of these references.

Claim 9 recites that, in the display screen as claimed in claim 1, wherein the control means (2, 10, 20, 30, 40, 42, 44, 46, 48, 50) include initialization means (50) for initializing the load capacitors (16, 26, 36) intended to discharge all the load capacitors connected to the modulation transistors of a column (claim 8), the initialization means (50) include an initialization transistor (50) having a gate electrode and two current-carrying electrodes, one current-carrying electrode of the said initialization transistor (50) being connected to the gate electrode of the modulation transistors (14, 24, 34) of the said column, the gate electrode of the said initialization transistor (50) being connected to a current-carrying electrode and to the addressing electrode (40) of a column of light emitters.

The Examiner indicated that Koyama et al. discloses everything claimed as applied above (see claim 8), in addition, Koyama et al. discloses wherein the initialization means include an initialization transistor having a gate electrode and two current-carrying electrodes, one current-carrying electrode of the said initialization transistor being connected to the gate electrode of the modulation transistors of the said column [reset TFT 117, figure 11], however, Koyama et al. fails to disclose "the gate electrode of the said initialization transistor being connected to a current-carrying electrode and to the addressing electrode of a column of light emitters".

In Lo, the gate electrode G of the initialization transistor T4 (FIGS. 1-3) is indeed connected to a current-carrying electrode D of this transistor, and to an electrode 111. However, instead of being an "addressing electrode of a column

of light emitters" as recited in claim 9, this electrode 111 is a so-called "previous scan line », which is definitely NOT an "addressing electrode" but a "scan electrode".

Therefore, Lo cannot teach the claimed invention, and claim 9 which depends on claim 1 is patentable over Koyama et al. in view of Lo.

Claim 10 recites that, in the display screen as claimed in claim 1, wherein the control means (2, 10, 20, 30, 40, 42, 44, 46, 48, 50) include initialization means (50) for initializing the load capacitors (16, 26, 36) intended to discharge all the load capacitors connected to the modulation transistors of a column (claim 8), the initialization means (50) include a diode, the cathode of which is connected to the gate electrode of the modulation transistors (14, 24, 34) and the anode of which is connected to the addressing electrode (40) of a column of light emitters.

In Lo, as the gate electrode G of the initialization transistor T4 (FIGS. 1-3) is connected to a current-carrying electrode D of this transistor, this initialization transistor T4 works indeed as a diode. But the current-carrying electrode D is connected an electrode 111, which is definitely NOT an "addressing electrode" but a "scan electrode" (see above).

Therefore, Lo cannot teach the claimed invention, and claim 10 which depends on claim 1 is patentable over Koyama et al. in view of Lo.

CONCLUSION

Thus, the applicants submit that none of the claims, presently in the application, are anticipated under the provisions of 35 U. S. C. § 102, or obvious under the provisions of 35 U. S. C. § 103. Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867, so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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